Hello, I am Jordan Ketteringham my supervisor is Prof C.J. Fourie and today I will be giving you an overview of my skripsie: The development of a basic but full gate library using AQFP cells for the development of complex multi-gates.

This overview is broken into three main goals first creating basic logic gates using AQFP technology. Secondly Using these basic AQFP logic gates to create more complex multi Gates

and finally testing the multi-gates using JoSim software to give a brief overview of what the design process looks like.

To start we will look at what AQFP technology is.

Adiabatic quantum flux parametrium or AQFP for short is a type of superconducting logic this logic operates at low temperatures near 0 Kelvin. At these temperatures superconducting metals experience a shift in state where they change from a state of electrical resistance to a state of no electrical resistance, this means superconducting metals can maintain an electrical current with no electrical losses.

the A in AQPF stands for adiabatic and describes the switching process of the system, AQFP technology switches slowly between states to allow the system to slowly evolve from one state to another while minimizing the energy dissipation this will be described further later on.

the Q in AQFP stands for quantum, which refers to the fundamental principles of quantum mechanics and describes the behavior of matter and energy at extremely small scales

Finally, the FP in in AQFP stands for flux parametron and refers to a specific method of processing quantum information using flux.

the Josephson junction is the building block of aqfp circuits. The Josephson junction is simply too superconducting materials separated by a thin insulating barrier. This is known as the SIS barrier or the superconducting insulator superconducting barrier. The SIS barrier allows for the phenomenon of quantum coherence to take place. This means the wave functions of electrons in the superconductors can extend into the insulator, allowing them to tunnel through the insulator without resistance. The SIS barrier is made into a superconducting loop which will allow a super current to flow indefinitely while a phase difference is maintained across the junction.

The figure shows the basic setup of a superconducting loop containing a JJ represented by the X. Inductors LX and L1 are coupled magnetically. LX carries the AC excitation current used to clock AQFP devices. This current produces a magnetic flux which then induces a single flux quanta in the superconducting loop. The result is a supercurrent that flows within the loop as long as the phase difference across the Josephson junction is maintained. By controlling the phase difference across the junction one can control the current in the superconducting loop.

The following slide shows how this loop is used to create the buffer. In this figure you can see the buffer is made from 2 superconducting loops each containing 1jj the inductors labeled LX and LD carry the AC excitation currents and the DC offset current. These inductors are coupled to inductors L1 and L2 and are used to power and clock all of the aqfp cells. Inductor Lin carries a DC input current and is used to determine whether a logical one or a logical 0 is output by the circuit.

In this diagram the current in Lin flows into the circuit which induces a current in the left superconducting loop this represents A logical one and will result in a large downward output current.

The following figure is the same but the input current is reversed, as a result the current is induced in the right superconducting loop which represents A logical 0 and results in a large upwards output current.

Next is the constant gate, it is designed similar to the buffer but without the need of an input inductor Lin. However, the output of this gate still needs to be predictable. To achieve this the value of inductor L1 is increased this results in an increased coupling factor between inductors Lx and L1 which means the circuit is biased towards the left loop and a single flux quanta is induced in the left superconducting loop. This represents a logical 1. This can be reversed, increasing L2 which would increase the mutual inductance between L2 and Lx and a sfq would induced in the right loop, representing a logical 0.

To power and clock all of the AQFP circuits two AC excitation signal runs in inductor LX. These signals are 90 degrees apart in phase and both have a frequency of 5GHz.

Logic gates at theta1 and theta 3 are clocked by the rising and falling edge of Ix1 and gates at theta 2 and theta 4 are clocked by the falling and rising edge of ix2.

Now we shall look at adiabatic switching within AQFP circuits. Adiabatic switching requires slow and controlled changes in the circuit parameters such as magnetic flux or bias current, this gives the junction enough time to evolve from one energy level to another without dissipating energy. This is why the excitation current in LX has a frequency of 5GHz. At this frequency the period is 200ps this means the rise time of the signal is 50ps which is enough time for the system to evolve from 1 state to another with minimal energy dissipation. Therefore, 5GHz optimal for processing speed while still greatly reducing the energy consumption.

This diagram is an example of an AND gate and will be used to describe the working of majority logic. Firstly, looking at the truth table it is important to note that majority logic cannot be changed, it simply takes the most prevalent input. We can only change its inputs to the system.

To create an AND gate we Force One of the inputs to a 0 which means we will only focus on the top half of the truth table this represents the logic of an AND gate where we see the output is only one when both inputs B&C are equal to 1. Similarly to the AND gate, by forcing one of the inputs to a 1 we can achieve the operation of the OR gate.

AND Gate example.

A problem faced with majority logic a problem faced with majority logic is when adding many signals the resultant output is often distorted therefore we always put the output of an AND gate through a buffer.

Next Slide

This is an example of an and gate output which is pretty unusable or unreadable until it is fed through a buffer where it produces the second output this output is more clear and becomes usable.

This is why NEXT SLIDE when creating complex multi gates such as the full adder we have to use so many buffers. Buffers are added at every intermediate step to ensure the signal is clear and readable. These buffers are also added to ensure the signal path length is always the same. This ensures signals arrive at logic gates at the same time. (Give example)